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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,502	11/07/2003	Gurpreet Bhullar	PAT 2445B-2-US	8548

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	**PAPER NUMBER**
2611	

MAIL DATE	DELIVERY MODE
07/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/702,502	BHULLAR ET AL.	
	Examiner	Art Unit	
	Kevin M. Burd	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. This office action, in response to the amendment filed 5/30/2007, is a final office action.

Response to Arguments

2. Applicant's arguments filed 5/30/2007 have been fully considered but they are not persuasive.

3. Applicant states the decoder element of claim 1 of the instant application is absent in claims 1-3 of Bhullar et al (US 6,683,928). The examiner disagrees. Claim 1 discloses the counter provides an output result for adjusting the number of fine delay elements in the first path. The counter acts as the decoder. In addition, the amendment to claim 1 claims the delay paths include a first plurality of delay elements and a second plurality of delay elements where all of the first plurality of delay elements and the second plurality of delay elements being active for delaying the clock signal. Bhullar discloses this limitation in claim 1. The first and second pluralities of delay elements claimed are the active delay elements. The delay elements that are not active are not a portion of the plurality of delay elements.

4. Applicant states the decoder element of claim 1 of the instant application is absent in claim 1 of Bhullar et al (US 6,327,318). The examiner disagrees. Claim 1 discloses the counter provides an output result to a circuit for applying the fine delay count to the controller for adjusting the number of fine delay elements in the first path. The circuit and controller act as the decoder. In addition, the amendment to claim 1 claims the delay paths include a first plurality of delay elements and a second plurality

of delay elements where all of the first plurality of delay elements and the second plurality of delay elements being active for delaying the clock signal. Bhullar discloses this limitation in claim 1. The first and second pluralities of delay elements claimed are the active delay elements. The delay elements that are not active are not a portion of the plurality of delay elements.

5. Applicant states the newly added limitation to the independent claims is not taught by Sloan et al (US 5,515,403). The examiner disagrees. Sloan discloses the active delay elements in the delay paths comprise a first and second plurality of delay elements. All of these pluralities of delay elements will be active. In addition, applicant states Sloan does not discloses that the microprocessor executes counter and decoder functionality analogous to those recited in claim 1. The examiner disagrees. Sloan discloses the microprocessor receives a phase difference signal and adjusts the delay. "A controller is coupled to the phase detector for controlling the delay values of the first and second delay paths to phase align the timing signals in response to a status signal " is stated in column 1, lines 48-52.

For these reasons and the reasons stated in the previous office action, the rejections of the claims are maintained and stated below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9, 13-21, 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Sloan et al (US 5,515,403).

Regarding claims 1-3, 8, 9, 13-15, 20, 21, 25 and 26, Sloan discloses a circuit comprising first and second parallel delay paths receiving a clock signal as shown in figure 8. Each of the delay paths comprises a delay stage where the delay stage comprises delay elements. The active delay elements in the delay paths comprise a first and second plurality of delay elements. All of these pluralities of delay elements will be active. A phase detector receives first and second clock delay signals from the first and second delay paths (figure 8). The phase detector provides the output of the phase detector, including phase lock status signals (column 6, lines 38-49) to a counter (microprocessor). A decoder (microprocessor) receives the phase lock status signals and uses the signals for storage and computational purposes (column 6, lines 38-49). The status signals also include UP/DOWN signals. Figure 16 shows the method of using the circuit. This includes an increment to the fine delay when the circuit is not phase locked (steps 556, 558, 560).

Regarding claims 4-7 and 16-19, the first delay path comprises a coarse delay stage 192 and the second delay path comprises a coarse delay stage 194 in addition to a fine delay stage 196.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-9, 13-21, 25 and 26 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 6,683,928. Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious for one of ordinary skill in the art at the time of the invention to remove components of the delay compensation circuit of Bhullar to minimize the size and complexity of the circuit.

8. Claims 1-26 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,327,318. Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious for one of ordinary skill in the art at the time of the

invention to remove components of the delay compensation circuit of Bhullar to minimize the size and complexity of the circuit.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

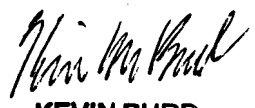
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kevin M. Burd
7/18/2007



KEVIN BURD
PRIMARY EXAMINER